

Methods of Suppression or Avoidance of Parallel-Plate Power Leakage from Conductor-Backed Transmission Lines

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Four useful methods are presented to suppress and/or avoid parallel-plate leakage from conductor-backed printed transmission lines. These include: 1) the use of shorting-pins; 2) the use of a dielectric-guide-coupled configuration; 3) using a two-layered conductor-backing configuration; and 4) dielectric loading on top. New analyses to model the leakage suppression due to the shorting-strips and the dielectric-guide-coupled geometries are presented, with selected demonstrative results and critical discussions. It is concluded that the unwanted leakage in many printed transmission lines, that are otherwise attractive for integrated circuits and phased array applications, can be successfully avoided and/or significantly suppressed using the proposed techniques.

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